REMARKS

Claims 1-10 are presented for examination. Independent claims 1 and 6 have been amended to more clearly define the claimed invention.

In particular, claim 1, as amended, recites a back annotation apparatus that includes:

-a pre-layout simulation implementing part for carrying out a pre-layout simulation to detect nodes of which the potential changes when a predetermined signal is applied to a logic circuit during the pre-layout simulation;

-a layout pattern verification implementing part for implementing a predetermined layout pattern verification for layout patterns of said logical circuit;

-a parasitic element extraction part connected to said pre-layout simulation implementing part which extracts parasitic elements from said nodes detected during the pre-layout simulation;

-a net list generation part connected to said parasitic element extraction part for generating a net list which includes all the devices included in layout pattern data and parasitic elements extracted in said parasitic element extraction part; and

-a post layout simulation implementing part connected to said net list generation part for implementing a post layout simulation by using said net list.

Claim 6, as amended, recites a back annotation method that includes:

-the step of performing a pre-layout simulation to detect nodes of which the potential changes when a predetermined signal is applied to a logic circuit during the pre-layout simulation;

-the step of implementing a predetermined layout pattern verification with respect to a layout pattern of said logic circuit;

-the step of extracting parasitic elements from said nodes detected during the pre-layout simulation;

-the step of generation of a net list including all the devices included in layout pattern data and the parasitic elements extracted in said step of extracting parasitic elements; and

-the step of implementation of a post layout simulation by using said net list.

Hence, the claims have been amended to stress that the claimed invention involves performing a pre-layout simulation to detect active nodes, i.e. nodes the potential of which changes when a predetermined signal is applied to a logic circuit during the pre-layout simulation.

Further, the invention involves performing extracting parasitic elements based on results of the pre-layout simulation. As discussed in the specification, this feature results in reducing the time required to perform extracting parasitic elements.

In addition, the invention involves performing a post-layout simulation using the netlist generated based on results of the pre-layout simulation. As discussed in the specification, this feature results in reducing the time required to perform the post-layout simulation.

It is noted that claims 1-10 stand rejected under 35 U.S.C. 102(e) as being anticipated by Ho.

In the previous responses, Applicant submitted that Ho does not teach the pre-layout simulation.

The Examiner took the position that Ho teaches a continuous net by net extraction that includes extracting node information after or before a potential change occurs at the node. The Examiner relies upon col. 5, lines 1-6 and 15-20 of the reference.

Considering the reference, Ho discloses a layout parasitic extraction system that involves Net-by-net R and C Extract 111 that extracts layout parasitics net by net (col.5, lines 3-5). However, Ho does not suggest the pre-layout simulation for detecting nodes of which the potential changes when a predetermined signal is applied to a logic circuit during the pre-layout simulation, as claims 1 and 6 require.

In the Advisory Action of April 27, 2005, the Examiner takes the position that the Net-by-Net R and C extraction step of Ho is dependent on the RC library. "Therefore, the Net-by-Net R and C extraction step can be done at any time including prior to the layout extraction step." The Examiner relies upon col. 5, lines 15-20 for supporting his position.

The Examiner position is respectfully traversed for the following reasons.

The reference discloses that "**in addition to a connectivity-based database**, Net-by-Net R and C extract 111 also utilizes RC library 109" (col. 5, lines 15-16). Further, Ho discloses that the connectivity-based database is created during Conversion 101 (col. 5, lines 2-3), which results in creating "a database where **geometries of the layout** are referenced according to the circuit schematic by net. " (col. 4, lines 35-38).

Accordingly, the connectivity-based database utilized for the Net-by-Net R and C extraction step 111 of Ho is created after the layout. Therefore, the Net-by-Net R and C extraction step 111 is also performed after the layout.

It is noted that even if the Examiner's position were correct, the reference still would not anticipate the claimed invention under 35 U.S.C. 102. Even assuming *arguendo* that the Ho's extraction step could be done before the layout step, it would not mean that the reference teaches or suggests performing the extracting step before the layout step.

Moreover, as clarified in the amended claims 1 and 6, the claimed invention requires extracting parasitic elements from the nodes detected during the pre-layout simulation. Hence, the claims require performing extraction of parasitic elements based on results of the pre-layout simulation.

Ho does not teach or suggest this feature.

Furthermore, Ho does not teach or suggest performing a post-layout simulation using the netlist generated based on results of the pre-layout simulation, as claims 1 and 6 require.

It is well settled that anticipation under 35 U.S.C. § 102 requires the disclosure in a single reference of each element of a claimed invention. ***Minnesota Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.***, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992).

As Ho does not disclose the claimed features discussed above, it does not anticipate the claimed invention within the meaning of 35 U.S.C. 102. Therefore, claims 1-10 are clearly defined over Ho.

In view of the foregoing, and in summary, claims 1-10 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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